AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Previously presented) A process for passivating a magneto-resistive bit structure characterized by the steps of:

providing a GMR stack upon a substrate;

selectively patterning said GMR stack to form at least one GMR bit having a top surface and side walls;

providing a conductive etch stop barrier layer that encapsulates the patterned GMR stack including the top surface and side walls of the GMR bit; and

selectively patterning said barrier layer so that the edges of the barrier layer extend out past the edges of the GMR bit.

9. (Original) The process as defined in Claim 8, further comprising forming a diffusion barrier between the etch stop barrier layer and the patterned GMR stack.

10. (Original) The process as defined in Claim 8, wherein selectively patterning the barrier layer further comprises:

forming a dielectric layer upon the barrier layer;

removing parts of the dielectric layer to expose portions of the barrier layer to be removed; and

ion milling to remove the exposed portions of the barrier layer to selectively pattern the barrier layer.

11. (Original) The process as defined in Claim 10, wherein removing comprises reactive ion etching.

12. (Original) A process for passivating a patterned magneto-resistive bit structure in a magneto-resistive memory, the process comprising:

providing a substrate with the patterned magneto-resistive bit structure, the patterned magneto-resistive bit structure having a top surface and side walls;

forming a conductive etch stop barrier layer over the substrate with the patterned magneto-resistive bit structure, the conductive etch stop barrier layer covering the top surface of the magneto-resistive bit structure and the side walls of the magneto-resistive bit structure; and

patterning the conductive etch stop barrier layer such that the conductive etch stop barrier layer is removed from portions of the substrate, but where the conductive etch stop barrier layer remains on the top surface and around the side walls of the magneto-resistive bit structure.

13. (Original) The process as defined in Claim 12, wherein the substrate further comprises a monolithic integrated circuit.

14. (Original) The process as defined in Claim 12, wherein the conductive etch stop barrier layer comprises CrSi.

15. (Original) The process as defined in Claim 14, wherein the conductive etch stop barrier layer is about 300 Å.

16. (Original) The process as defined in Claim 12, further comprising:

forming a diffusion barrier before forming the conductive etch stop barrier layer such that the diffusion barrier is formed between the conductive etch stop barrier layer and the substrate with the patterned magneto-resistive bit structure; and

wherein patterning the conductive etch stop barrier layer further comprises patterning the diffusion barrier.

17. (Original) The process as defined in Claim 16, wherein the diffusion barrier comprises Ta.

18. (Original) The process as defined in Claim 17, wherein the diffusion barrier is about 100 Å in thickness.

19. (Original) The process as defined in Claim 16, wherein the diffusion barrier comprises TaN.

20. (Original) The process as defined in Claim 12, further comprising:

forming a diffusion barrier comprising Ta before forming the conductive etch stop barrier layer such that the diffusion barrier is formed between the conductive etch stop barrier layer and the substrate with the patterned magneto-resistive bit structure, wherein the conductive etch stop barrier layer comprises CrSi, and wherein the substrate further comprises a monolithic integrated circuit; and

wherein patterning the conductive etch stop barrier layer further comprises patterning the diffusion barrier.